1. A method comprising:

forming a buried line of a first conductive type in a substrate, said buried line including a pair of more lightly doped regions around a more heavily doped region;

creating a region of a second conductivity type opposite said first conductivity type over said line; and

forming a phase-change material over said region.

2. The method of claim 1 including forming a passage through a dielectric layer.

3. The method of claim 2 including forming a contact layer under said dielectric layer and forming said passage through said dielectric layer to said contact layer.

4. The method of claim 3 including forming the phase-change material in said passage.

5. The method of claim 1 including forming a buried line wherein said lightly doped regions reduce the reverse bias leakage of said line.

6. The method of claim 5 including forming said more lightly doped regions using ion implantation.

7. The method of claim 1 including forming a pair of trenches on either side of said buried line.

8. The method of claim 1 wherein forming a buried line includes forming a buried wordline.

9. The method of claim 1 including forming said more lightly doped regions of N type material.

10. The method of claim 9 including forming a P type region over said buried line and forming said buried line in a P type substrate.

11. A memory cell comprising:

a substrate;

a phase-change material over said substrate;

a buried line of a first conductivity type in said substrate, said buried line including a pair of more lightly doped regions around a more heavily doped region; and

a region of a second conductivity type opposite said first conductivity type over said line and under said phase-change material.

12. The memory cell of claim 11 including a dielectric material defining a pore over the substrate, said phase-change material being formed in said pore.

13. The memory cell of claim 12 including a contact layer under said dielectric layer aligned with said pore.

14. The memory cell of claim 13 wherein said lightly doped regions reduce the reverse bias leakage of said line.

15. The memory cell of claim 13 including a pair of trenches on either side of said buried line.

16. The memory cell of claim 11 wherein said line is a wordline that couples to other memory cells.

17. The memory cell of claim 11 wherein said lightly doped regions are N-type material.

18. The memory cell of claim 17 wherein said lightly doped regions are N- regions.

19. The memory cell of claim 18 wherein said substrate is a P-type substrate.

20. The memory cell of claim 12 wherein said pore is lined with a sidewall spacer.

21. An electronic device comprising:

a surface;

a phase-change material over said surface; and

a conductive line in said surface having a more heavily doped region sandwiched between more lightly doped regions, said conductive line providing signals to said phase-change material.

22. The device of claim 21 wherein said phase-change material forms a memory cell of a storage.

23. The device of claim 22 wherein said storage is part of a computer.

24. The device of claim 22 including a processor, an interface and a bus coupled to said storage.

25. The device of claim 22 wherein said conductive line is a buried wordline.

26. The device of claim 25 including a conductive material between said phase-change material and said conductive line.

27. The device of claim 26 wherein said conductive line is formed of a material having a first conductivity type, a material of a second conductivity type being defined in said surface over said conductive line.

28. The device of claim 27 wherein said more heavily doped region is an N+ region and said more lightly doped regions are N- regions.

29. The device of claim 21 wherein said surface includes a semiconductor substrate.

30. The device of claim 29 including an insulator material positioned over said surface and a pore being formed in said insulator material, said phase-change material being formed in said pore.